REMARKS:

Applicant notes with appreciation that claims 7-11 have been allowed. Claims 1-14 and 21-26 are pending. Claims 2-8, 13, and 14 have been amended to correct for formalities including antecedent basis, and typographical and grammatical errors. Support for new claims 21 and 25 is found, *inter alia*, in originally filed claim 2. Support for new claims 22 and 26 is found, *inter alia*, in originally filed claim 3. Support for new claim 23 is found, *inter alia*, in originally filed claim 4. Support for new claim 24 is found, *inter alia*, in originally filed claim 5. Applicant has amended the specification to correct for typographical errors. Also, applicant has amended the Summary Of The Invention section of the specification to reflect amended claims 2-8, 13, and 14, and previously deleted claims 15-20. In addition, applicant has amended the Abstract Of The Disclosure section to reflect claim 12. No new matter has been added. Reexamination and reconsideration of the application, as amended, are respectfully requested.

On page 2 of the Office Action, the Examiner states: "The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed." Applicant has amended the title of the invention to be clearly indicative of the invention to which the claims are directed.

Also on page 2 of the Office Action, the Examiner states: "Figures 6-9 should be designated by a legend such as - - Prior Art - - because only that which is old is illustrated." In response, applicant has amended Figs. 6-9 by adding the designation "(PRIOR ART)" as indicated in red ink on attached copies thereof.

On pages 2-3 of the Office Action, the Examiner rejects claims 1-3 and 12 under 35 U.S.C. § 102(e) as being anticipated by or, in the alternative, under 35 U.S.C. § 103(a) as being obvious over Mehta (USP 6,362,527). Anticipation requires that each and every element as set forth in the claims be found in a single prior art reference. *Verdegaal Bros., Inc. v. Union Oil Co. of California*, 814, F.2d 628, 631, 2

U.S.P.Q.2d (BNA) 1051, 1053 (Fed. Cir. 1987). A prima facie obviousness rejection requires that the prior art reference, or references, when combined, must teach all of the claim limitations. MPEP § 2143.03; In re Fine, 837 F.2d 1071, 5 U.S. P.Q.2d (BNA) 1596 (Fed. Cir. 1988). Applicant respectfully traverses these rejections to claims 1-3 and 12.

Claim 1 recites a semiconductor device having a wiring pattern that is formed by etching a conductive layer using a resist pattern as a mask. The semiconductor device includes a contact section, a first wiring, and a second wiring. The contact section is formed in an interlayer dielectric layer. The first wiring is formed over the interlayer dielectric layer and disposed with a separation from the contact section shorter than a specified separation. The second wiring has a connection region to be connected to the contact section. The second wiring has an extension section extending in a non-wiring region in the connection region to be connected to the contact section. The extension section is disposed in at least one section of the connection region other than sides thereof facing the first wiring.

Claim 12 recites a semiconductor device having a wiring pattern formed by etching a conductive layer using a resist pattern as a mask. The semiconductor device includes a contact section and a wiring. The contact section is formed in an interlayer dielectric layer. The wiring has a connection region to be connected to the contact section. The connection region of the wiring has a generally square plan configuration. The wiring has an extension section extending in a non-wiring region in the connection region.

Applicant submits that independent claims 1 and 12 are patentable over Mehta because Mehta does not teach or suggest, "a first wiring formed over the interlayer dielectric layer and disposed with a separation from the contact section shorter than a specified separation . . . wherein the second wiring has an extension section extending in a non-wiring region in the connection region to be connected to

the contact section, and the extension section is disposed in at least one section of the connection region other than sides thereof facing the first wiring," as required by claim 1 or, "wherein the connection region of the wiring has a generally square plan configuration, and the wiring has an extension section extending in a non-wiring region in the connection region," as required by claim 12. On page 3 of the Office Action, the Examiner states:

> Mehta, in Fig. 2D, discloses a semiconductor device having a wiring pattern, the semiconductor device comprising: a contact section 14 formed in an interlayer dielectric layer; a first wiring 6 (left wiring) formed over the interlayer dielectric layer and disposed with a separation from the contact section shorter than a specified separation; and a second wiring 6 (right wiring) having a connection region to be connected to the contact section 14, wherein the connection region of the wiring 6 has a generally square plan configuration, the second wiring 6 has at least one extension section extending in a non-wiring region and disposed in at least one section of the connection region other than sides thereof facing the first wiring.

However, as discussed in column 5, lines 53-67, the metal lines 6 in Fig. 2D *underlie* the vias 14. Therefore, Mehta does not teach, "a first wiring formed *over* the interlayer dielectric layer . . . ." (Emphasis added). Also, Mehta makes no mention of, "a separation from the contact section shorter than a specified separation." In contrast, Mehta is concerned with minimum border requirements of the metal lines 6 that surround each via 14.

Mehta's Fig. 2D teaches curved portions metal lines 6 that project away from the vias 14 on both sides. If the curved region of the metal line 6 that surrounds each via 14 in Mehta constitutes, "the connection region," required by claims 1 and 12, then Mehta does not teach or suggest a wiring having a separate, "extension section extending in a non-wiring region in the connection region . . . ." Even if the curved region of the metal line 6 were erroneously construed to be both the connection region and an extension section, the curved region of the metal line 6,

defined by the Examiner as the "right wiring," that surrounds via 14 projects toward the other metal line 6, defined by the Examiner as "left wiring." Thus, Mehta teaches against, "the extension section is disposed . . . other than sides thereof facing the first wiring."

Thus, Mehta does not teach or suggest, "a first wiring formed over the interlayer dielectric layer and disposed with a separation from the contact section shorter than a specified separation . . . wherein the second wiring has an extension section extending in a non-wiring region in the connection region to be connected to the contact section, and the extension section is disposed in at least one section of the connection region other than sides thereof facing the first wiring," or, "wherein the connection region of the wiring has a generally square plan configuration, and the wiring has an extension section extending in a non-wiring region in the connection region."

Accordingly, applicant submits that independent claims 1 and 12, and depending claims 2-6, 13, and 14, are neither anticipated nor taught or suggested by Mehta, but rather are patentable thererover.

On page 3 of the Office Action, the Examiner rejects claims 12-14 under 35 U.S.C. § 102(e) as being anticipated by or, in the alternative, under 35 U.S.C. § 103(a) as being obvious over Geryk (USP 6,166,441). Applicant respectfully traverses these rejections to claims 12-14.

Applicant submits that independent claim 12 is patentable over Geryk because Geryk does not teach or suggest, "wherein the connection region of the wiring has a generally square plan configuration, and the wiring has an extension section extending in a non-wiring region in the connection region," as required by claim 12. On page 3 of the Office Action, the Examiner states:

> Geryk, in Fig. 5, discloses a semiconductor device having a wiring pattern, the semiconductor device comprising: a contact section formed over an interlayer dielectric layer; and a wiring 550 having a

connection region to be connected to the contact section, wherein the connection region of the wiring has a generally square plan configuration, the wiring has extension sections on four sides of the connection region and at least one of the extension sections extending in a non-wiring region in the connection region.

Fig. 5 in Geryk only teaches a metal trace 550 and an octagonal overlap 520 over a square via. If the octagonal overlap 520 that covers the via in Geryk constitutes, "the connection region," required by claim 12, then Geryk does not teach or suggest a wiring having a separate, "extension section extending in a non-wiring region in the connection region . . . ." Thus, Geryk does not teach or suggest, "wherein the connection region of the wiring has a generally square plan configuration, and the wiring has an extension section extending in a non-wiring region in the connection region."

Accordingly, applicant submits that independent claim 12, and depending claims 13 and 14, are neither anticipated nor taught or suggested by Geryk, but rather are patentable thererover.

On page 4 of the Office Action, the Examiner rejects claims 1-6 and 12 under 35 U.S.C. § 103(a) as being unpatentable over Bush et al. (USP 6,380,554) in view of Fulford, Jr. et al (USP 5,916,715). Applicant respectfully traverses these rejections to claims 1-6 and 12.

Applicant submits that independent claims 1 and 12 are patentable because neither Bush nor Fulford teach or suggest, "a contact section formed in an interlayer dielectric layer; a first wiring formed over the interlayer dielectric layer and disposed with a separation from the contact section shorter than a specified separation . . . wherein the second wiring has an extension section extending in a non-wiring region in the connection region to be connected to the contact section, and the extension section is disposed in at least one section of the connection region other than sides thereof facing the first wiring," as required by claim 1 or, "a contact

section formed in an interlayer dielectric layer . . . wherein the connection region of the wiring has a generally square plan configuration, and the wiring has an extension section extending in a non-wiring region in the connection region," as required by claim 12.

On page 4 of the Office Action, the Examiner states:

> Bush, in Fig. 3, discloses a semiconductor device having a wiring pattern, the semiconductor device comprising: a contact section 54 . . . ; a first wiring 72a disposed with a separation from the contact section shorter than a specified separation; and a second wiring 52 having a square connection region to be connected to the contact section, wherein the second wiring 52 has an extension section extending in a non-wiring region and disposed in at least one section of the connection region other than sides thereof facing the first wiring 72a, and wherein the extension section has an extension length identical with the width of the wiring. Bush does not disclose the contact section formed in an interlayer dielectric layer.

However, Bush makes no mention of, "a separation from the contact section shorter than a specified separation." In addition to not disclosing, "a contact section formed in an interlayer dielectric layer," as acknowledged by the Examiner on page 4 of the Office Action, Bush also does not teach or suggest, "a connection region to be connected to the contact section," much less an, "extension section extending in a non-wiring region in the connection region . . . ," or an, "extension section . . . disposed in at least one section of the connection region other than sides thereof facing the first wiring."

The Examiner cites Fulford merely for showing a, "contact section 10 formed in the dielectric layer 12 as taught in Figs. 3b and 4a of Fulford." However, neither Bush, as discussed above, nor Fulford teach or suggest, "a contact section formed in an interlayer dielectric layer; a first wiring formed over the interlayer dielectric layer and disposed with a separation from the contact section shorter than a specified separation . . . wherein the second wiring has an extension section

extending in a non-wiring region in the connection region to be connected to the contact section, and the extension section is disposed in at least one section of the connection region other than sides thereof facing the first wiring," or, "a contact section formed in an interlayer dielectric layer . . . wherein the connection region of the wiring has a generally square plan configuration, and the wiring has an extension section extending in a non-wiring region in the connection region."

Accordingly, applicant submits that neither Bush nor Fulford, nor the combination of Bush and Fulford, teach or suggest all of the requirements of independent claims 1 and 12. Therefore, independent claims 1 and 12, and depending claims 2-6, 13, and 14, are patentable over the cited references.

The art made of record but not relied upon by the Examiner has been considered. However, it is submitted that this art neither describes nor suggests the presently claimed invention.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6700 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: September 16, 2002

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Version with Markings to Show Changes Made

In the specification:

Page 3, line 25, through page 8, line 21, the section of the specification entitled SUMMARY OF THE INVENTION:

SUMMARY OF THE INVENTION

[It is an object of the present invention to provide a semiconductor device that provides a low contact resistance between wirings and contact sections embedded in connection holes and a high wiring reliability, and a method for manufacturing the same.

]In accordance with the present invention, a semiconductor device that has a wiring pattern that is formed by etching a conductive layer using a resist pattern as a mask [comprises]includes

a contact section formed in an interlayer dielectric layer,

a first wiring formed over the interlayer dielectric layer and disposed with a separation from the contact section shorter than a specified separation, and

a second wiring having a connection region to be connected to the contact section,

wherein the second wiring has an extension section extending in a non-wiring region in the connection region to be connected to the contact section, and

the extension section is disposed in at least one section of the connection region other than sides thereof facing the first wiring.

In the semiconductor device in accordance with the present invention, since the extension section is provided in the connection region to be connected to the contact section, the connection region of the wiring can almost completely cover the contact section in the lower layer. Therefore, the contact resistance between the contact section formed in the connection hole (contact hole or via hole) and the wiring can be made small, the wiring reliability can be improved.

A variety of embodiments may be provided for the semiconductor device of the present invention as described below. These embodiments are applicable to semiconductor devices having structures to be described below.

(a) The separation is shorter than a specified separation and there is a minimum separation between wirings in a wiring pattern (hereafter referred to as a "minimum inter-wiring separation"). The minimum inter-wiring separation may vary depending on the design rules, and may be, for example, 0.1 μm or greater but 1 μm or smaller.

(b) The connection region is square in its plan configuration having [generally the same diameter as that of the contact section, or square in its plan configuration having a diameter greater than that]dimensions that are greater than or equal to dimensions of the contact section.

(c) The extension section may preferably have the same width as the width of the wiring, and may preferably have the same extension length as the width of the wiring. Also, the extension section may preferably be square in its plan configuration.

Furthermore, semiconductor device in accordance with the present invention can have the following structures.

(1) A semiconductor device [comprises]includes

a contact section formed in an interlayer dielectric layer,

a first wiring formed over the interlayer dielectric layer and disposed with a minimum inter-wiring separation with respect to the contact section, and

a second wiring having a connection region to be connected to the contact section and extending in parallel with the first wiring,

wherein the connection region of the second wiring has a generally square plan configuration,

the second wiring has an extension section extending in a non-wiring region in the connection region, and

the extension section is disposed on sides of the connection region other than sides thereof facing the first wiring.

(2) A semiconductor device [comprises]includes

a contact section formed in an interlayer dielectric layer,

a first wiring formed over the interlayer dielectric layer and disposed with a minimum inter-wiring separation with respect to the contact section, and

a second wiring having a connection region to be connected to the contact section and extending in a direction perpendicular to the first wiring,

wherein the connection region of the second wiring has a generally square plan configuration,

the second wiring has an extension section extending in a non-wiring region in the connection region, and

the extension section is disposed on sides of the connection region other than sides thereof facing the first wiring.

(3) A semiconductor device [comprises]includes

a contact section formed in an interlayer dielectric layer,

a first wiring formed over the interlayer dielectric layer and disposed with a minimum inter-wiring separation with respect to the contact section, and

a second wiring having a connection region to be connected to the contact section and having a section extending in parallel with the first wiring and a section extending in a direction perpendicular to the first wiring,

wherein the connection region of the second wiring has a generally square plan configuration,

the second wiring has an extension section extending in a non-wiring region in the connection region, and

the extension section is disposed on sides of the connection region other than sides thereof facing the first wiring.

(4) A semiconductor device [comprises]includes

a contact section formed in an interlayer dielectric layer,

a first wiring formed over the interlayer dielectric layer and disposed with a minimum inter-wiring separation with respect to the contact section, and

a second wiring having only a connection region to be connected to the contact section,

wherein the connection region of the second wiring has a generally square plan configuration,

the second wiring has an extension section extending in a non-wiring region in the connection region, and

the extension section is disposed on sides of the connection region other than sides thereof facing the first wiring.

(5) A semiconductor device [comprises]includes

a contact section formed in an interlayer dielectric layer,

a plurality of first wirings formed over the interlayer dielectric layer and disposed with a minimum inter-wiring separation with respect to the contact section, and

a second wiring having at least one connection region to be connected to the contact section,

wherein the connection region of the second wiring has a generally square plan configuration,

the second wiring has an extension section extending in a non-wiring region in the connection region, and

the extension section is disposed on sides of the connection region other than sides thereof facing the plurality of first wirings.

(6) A semiconductor device [comprises]includes

a contact section formed in an interlayer dielectric layer, and

a wiring having a connection region to be connected to the contact section,

wherein the connection region of the wiring has a generally square plan configuration, and

the wiring has an extension section extending in a non-wiring region in the connection region.

[In this semiconductor device, the wiring may be in a line-like shape, and may have extension sections on three sides of the connection region. Also, the wiring may be formed from the connection region and may have extension sections on four sides of the connection region.

A manufacturing method in accordance with the present invention includes a first step of forming a mask pattern by disposing line patterns, setting a connection region pattern that at least covers a connection hole pattern in a lower layer, disposing extension patterns on sides of the connection region pattern, and erasing those of the extension patterns that face the line patterns with a separation shorter than a specified separation between the sides of the connection region pattern and adjacent ones of the line patterns,

a second step of forming a resist pattern on a conductive layer by lithography using the mask pattern, and

a third step of forming wiring patterns by etching the conductive layer using the resist pattern as a mask.

The manufacturing method in accordance with the present invention may have the following embodiments.

(a) The separation shorter than a specified separation is a minimum separation between lines in a line pattern.

(b) The connection region pattern is square having generally the

same size as that of the connection hole pattern, or square having a size greater than that of the connection hole pattern.

(c) The extension pattern may preferably have the same width as the width of a line of the line patterns, and may preferably have the same extension length as the width of a line of the line patterns. Also, the extension pattern may preferably be square.]

Page 1, line 11:

[DESCRIPTION OF RELATED TECHNOLOGY]BACKGROUND OF THE INVENTION

Page 10, lines 8-9:

DETAILED DESCRIPTION OF [PREFERRED EMBODIMENTS OF]THE INVENTION

Page 13, lines 22-29:

In the example shown in the figure, a first wiring 17 is disposed separated from the contact sections 36 and 46 by a separation shorter than a specified separation (about a minimum inter-wiring separation in this example). A second wiring 15 and the third wiring 16 are disposed in proximity to the first [wring]wiring 17. The first and second wirings 17 and 15 both extend in the X direction, and a third wiring 16 extends in the Y direction. Also, the second and third wirings 15 and 16 are disposed separated from the first wiring 17 by a minimum inter-wiring separation.

Page 17, lines 21-30:

In the example shown in the figure, a first wiring 17 is disposed separated from the contact sections 36 and 46 by a separation shorter than a specified separation (about a minimum inter-wiring separation in this example). A second wiring 31 and a third wiring 32 are disposed in proximity to the first [wring]wiring 17. The first wiring 17 extends in the X direction, and the second wiring 31 extends in the X direction and the Y direction. The third wiring 32 is composed only of a contact region for connecting upper and lower contact sections. Also, the second and third wirings 31 and 32 are disposed separated from the first wiring 17 by a minimum inter-wiring separation.

Page 33, lines 1-12, the section of the specification entitled ABSTRACT:

ABSTRACT

A semiconductor device has a [contact section formed in an interlayer dielectric layer, a first wiring formed over the interlayer dielectric layer and disposed with a separation from the contact section shorter than a specified separation, and a second wiring having a connection region to be connected to the contact section. The connection region has a shape that covers at least the contact section and preferably has a square shape. The second wiring has extension sections extending in non-wiring regions in the connection region to be connected to the contact section. The extension sections are disposed on sides of the connection region other than sides thereof facing the first wiring.]wiring pattern formed by etching a conductive layer using a resist pattern as a mask. The semiconductor device includes a contact section and a wiring. The contact section is formed in an interlayer dielectric layer. The wiring has a connection region to be connected to the contact section. The connection region of the wiring has a generally square plan configuration. The wiring has an extension section extending in a non-wiring region in the connection region.

In the claims:

2. (Amended) [A]The semiconductor device according to claim 1, wherein the separation is shorter than a specified separation and there is a minimum separation between wirings in the wiring pattern.

3. (Amended) [A]The semiconductor device according to claim 1, wherein the connection region is square in its plan configuration having [generally an identical diameter of the contact section, or square in its plan configuration having a diameter greater than that]dimensions that are greater than or equal to dimensions of the contact section.

4. (Amended) [A]The semiconductor device according to claim 1, wherein the extension section has an identical width as a width of the wiring.

5. (Amended) [A]The semiconductor device according to claim 1, wherein the extension section has an extension length identical with the width of the wiring.

6. (Amended) [A]The semiconductor device according to claim 1, wherein the extension section is square in its plan configuration.

7. (Amended) A semiconductor device having a wiring pattern formed by etching a conductive layer using a resist pattern as a mask, the semiconductor device comprising:

a contact section formed [over]in an interlayer dielectric layer;

a first wiring formed over the interlayer dielectric layer and disposed with a minimum inter-wiring separation with respect to the contact section; and

a second wiring having a connection region to be connected to the contact section and extending in parallel with the first wiring,

wherein the connection region of the second wiring has a generally square plan configuration,

the second wiring has an extension section extending in a non- wiring region in the connection region, and

the extension section is disposed on sides of the connection region other than sides thereof facing the first wiring.

8. (Amended) A semiconductor device having a wiring pattern formed by etching a conductive layer using a resist pattern as a mask, the semiconductor device comprising:

a contact section formed in an interlayer dielectric layer;

a first wiring formed over the interlayer dielectric layer and disposed with a minimum inter-wiring separation with respect to the contact section; and

a second wiring having a connection region to be connected to the contact section and extending in a direction perpendicular to the first wiring,

wherein the connection region of the second wiring has a generally square plan configuration,

the second wiring has an extension section extending in a non-wiring region in the connection region, and

the extension section is disposed [in]<u>on</u> sides of the connection region other than sides thereof facing the first wiring.

13. (Amended) [A]<u>The</u> semiconductor device according to claim 12, wherein the wiring is [in a]line-like <u>in</u> shape and has extension sections on three sides of the connection region.

14. (Amended) [A]The semiconductor device according to claim 12, wherein the wiring is formed from the connection region and [have]has extension sections on four sides of the connection region.

Fig. 5

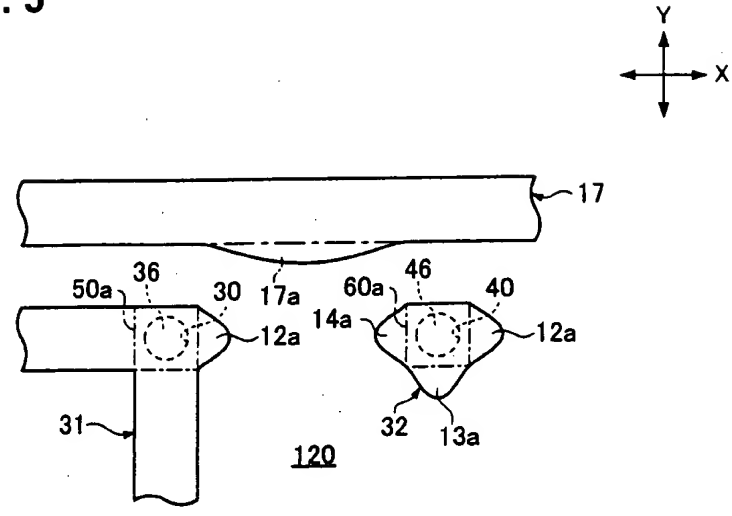
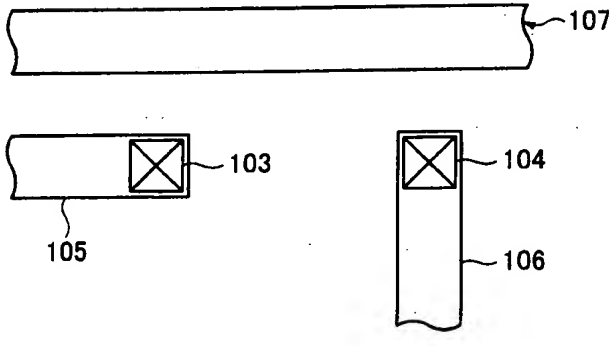


Fig. 6



(PRIOR ART)

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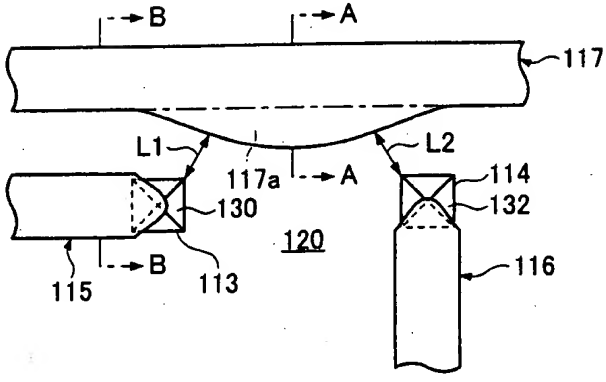
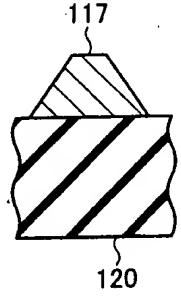
PC
12/2/02

Fig. 7



(PRIOR ART)

Fig. 8



(PRIOR ART)

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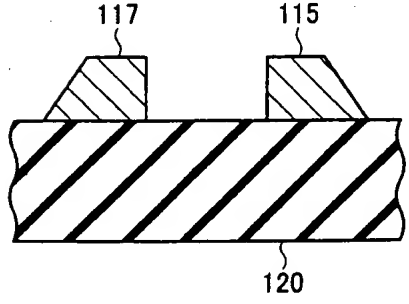
Fig. 9



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